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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,225	07/31/2003	Thomas McDonald	CNTR.2143	2075

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EXAMINER
MOLL, JESSE R

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/632,225	MCDONALD, THOMAS
	Examiner	**Art Unit**
	Jesse R. Moll	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>31 July 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-24</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-16 and 18-24</u> is/are rejected.

7)☒ Claim(s) <u>17</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>31 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
AU 2181
3/20/2006

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>31 July 2003</u>. 7/11/05, 9/26/05, 10/24/05

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-24 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS on July

31, 2003, IDS on July 11, 2005, IDS on September 28, 2005, and IDS on November 20,

2005. The papers filed have been placed on record.

Specification

2.   The specification is objected to because in paragraph [0002], the information

about co-pending applications is not up to date. Examiner requests that the application

numbers be inserted in lieu of the docket information.

Claim Rejections - 35 USC § 101

3.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

4.   Claim 24 is rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter.

Claim 24 recites the limitation "a computer data signal embodied in a transmission

medium". A computer data signal embodied in a transmission medium does not fall

under any of the statutory classes. First, a claimed signal is clearly not a "process"

under Sec. 101 because it is not a series of steps. The other three Sec. 101 classes of

machine, compositions of matter and manufactures "relate to structural entities and can

be grouped as 'product' claims in order to contrast them with process claims." 1 D.

Chisum, Patents Sec. 1.02 (1994). The three product classes have traditionally required

physical structure or material.

Examiner suggests (and assumes for the purpose of examination) that the

limitation "A computer data signal embodied in a transmission medium" read "A

computer program embodied on a computer readable medium". The term computer

usable (e.g., readable) medium as defined in Applicant's specification (page 46, lines

24-27) does not include non-tangible signals.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-15 and 19-24 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Eberly (The Correlation Branch Target Address Cache) in view of

Johnson (U.S. Patent No. 6,321,321).

7.   Regarding claim 1, Eberly discloses an apparatus for invalidating a redundant

entry for the same branch instruction in a branch target address cache (BTAC), the

apparatus comprising: a status indicator,

Note that since entries are invalidated, there must be a indication that these

entries exist.

for indicating whether at least two entries of the BTAC (see page 85, last 5 lines)

Note that when a branch is added, logic checks to see if another entry matches

the address tag. The logic checks if one matches (there are more than one valid entries

in the BTAC including the one just added).

selected by an instruction cache fetch address (the fetch address of the branch

instruction corresponding to the newly added entry in the BTAC; see page 84, last 2

lines)

Note that when entries are added to the BTAC, the entries contain a tag

(instruction fetch address of that branch instruction). The address of the branch

instruction is considered to be an instruction cache fetch address.

contain a valid branch target address (instructions only can be invalidated) for a

same branch instruction; and control logic (any circuitry which invalidates entries),

coupled to said status indicator (this control logic must receive this information in order

to invalidate those entries), for invalidating one of said at least two entries if said status

indicator indicates at least two ways of said selected set contain a valid branch target

address for a same branch instruction (see page 85, last 5 lines).

Note that if two entries are for the same branch instruction they will have the same address tag. Further note that any entry with a CTR bit different than the one currently being written for that tag will be invalidated.

Eberly does not expressly disclose that the BTAC is set associative or that entries in the BTAC are divided into sets and ways.

Johnson teaches the use of a set associative cache (see col. 2, lines 30-32) with multiple sets (see col. 2, lines 30-32), further split into multiple ways (see col. 2, lines 33-36).

For the combination to have been successful, redundant entries (entries for the same instruction) would inherently be grouped into the same set because their fetch addresses are equal.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Eberly by using a set associative BTAC with multiple ways and sets, as taught by Johnson, in order to decrease access time (see col. 1, last 2 lines, and col. 2, first 3 lines; col. 2, lines 42-44) and increase cache capacity (see col. 2, lines 2-5).

8.   Regarding claim 2, Eberly/Johnson discloses the apparatus of claim 1, further comprising: a register, coupled to said control logic, for storing said instruction cache fetch address, for use by said control logic to invalidate said one of said at least two ways of said selected set (two entries; see above regarding claim 1).

Note that since the information is used by the control logic to invalidate instructions, there must be something to store the information which is accessed by the control logic. Whatever stores the information is considered to be a register which is coupled to the control logic. Further note that the definition of register according to The American Heritage College Dictionary fourth edition is "A part of the central processing unit used as a storage location". Further note that even if the information is stored for less than a clock cycle, it still can be considered a register.

9.   Regarding claim 3, Eberly/Johnson discloses the apparatus of claim 1, wherein said selected set is selected by an index portion of said instruction cache fetch address.

Johnson shows that in set associative caches, sets are selected with an index portion of the read address (see col. 2, lines 20-23 and 30-35). Therefore, any combination modifying the invention of Eberly by using a set associative cache would select a set by using an index portion of said fetch address.

10.   Regarding claim 4, Eberly/Johnson discloses the apparatus of claim 1, wherein said control logic clears said status indicator after invalidating said one of said at least two ways (entries, see above regarding claim 1) of said selected set.

Note that since the status indicator indicates duplicate entries, when the duplicate entries are removed, the status indicator would no longer be set.

11.   Regarding claim 5, Eberly/Johnson discloses the apparatus of claim 1, further

comprising: a register, coupled to said control logic, for storing data specifying said one

of said at least two ways (two entries) of said selected set to invalidate, for use in

invalidating said one of said at least two ways of said selected set (two entries with the

same address must have the same set).

Note that since the information must be known to the control logic in order to

invalidate the entries, there must be something to store the information. Whatever

stores this information is considered to be the register.

12.   Regarding claim 6, Eberly/Johnson discloses the apparatus of claim 1, further

comprising: at least two valid signals (see page 84, 4th paragraph, first 2 lines), coupled

to said control logic, each for indicating whether a respective one of said at least two

ways (entries) of said selected set contain a valid branch target address (valid bits are

used to keep track of entry validity).

Further note that claim 12 recites equivalent limitations as claim 6 and is

therefore rejected under the same grounds.

13.   Regarding claim 7, Eberly/Johnson discloses the apparatus of claim 1, further

comprising: at least two match signals, coupled to said control logic, each for indicating

whether a tag portion of said instruction cache fetch address matches a tag stored in a

respective one of said at least two ways (entries) of said selected set (see page 85, last

2 lines regarding invalidating all entries with the same address tag and CTR bit = 1.).

Note that by saying all entries are invalidated implies that there can be more than

1. Therefore, the logic checks more than 1 entry.   Further note that since the control

logic invalidates these entries, there must be a signal showing that the addresses match

the address of the entry that was added.

14.   Regarding claim 8, Eberly/Johnson discloses the apparatus of claim 7, further

comprising: at least two comparators, coupled to said control logic, each for comparing

said tag portion of said instruction cache fetch address with said tag stored in said

respective one of said at least two ways (entries) of said selected set, and generating a

respective one of said at least two match signals in response to said comparing.

Note that the signal to show a match must be created by some hardware. The

hardware is considered to be the at least two comparators (one for each entry).

Further note that claim 11 recites equivalent limitations as claim 8 and is

therefore rejected under the same grounds.

15.   Regarding claim 9, Eberly/Johnson discloses an apparatus for invalidating

redundant entries for the same branch instruction in a branch target address cache

(BTAC), comprising: detection logic (any circuitry which detects two entries with the

same address), for detecting a condition in which more than one valid way of a plurality

of ways of a selected set of the BTAC are storing a target address for a same branch

instruction (see page 85, last 5 lines);

Note that if two entries are for the same branch instruction they will have the

same address tag.

And invalidation logic (any circuitry which invalidates entries), coupled to said

detection logic, for invalidating all but one of said more than one valid way of said

selected set (see page 85, last 5 lines).

Note that any entry with a CTR bit different than the one currently being written

for that tag will be invalidated if the two entries share the same address.

16.   Regarding claim 10, Eberly/Johnson discloses the apparatus of claim 9, further

comprising: a register, coupled to said invalidation logic (see above regarding claim 2),

for storing an instruction cache fetch address (the fetch address of the branch

instruction corresponding to the newly added entry in the BTAC; see page 84, last 2

lines); wherein said selected set is selected by an index portion of said instruction cache

fetch address (tag of instruction added to BTAC), wherein said invalidation logic

invalidates said all but one of said more than one valid ways (entries) of said selected

set using said instruction cache fetch address stored in said register (see page 85, last

5 lines).

Note that if the CTR bit of the newly added item differs from the entries currently

in the BTAC, all entries besides the newly added entry are invalidated.

17.   Regarding claim 13, Eberly/Johnson discloses the apparatus of claim 12, further

comprising: a flag, coupled to said detection logic, for indicating whether more than one

valid way of a plurality of ways of a selected set of the BTAC are storing a target

address for a same branch instruction (see page 85, last 5 lines),

Note that the invalidation logic invalidates entries based on information from the

detection logic. This must include information to determine if an entry is to be

invalidated. This information is considered to be the flag.

wherein said detection logic sets said flag to a true value if for more than one of

said plurality of ways said match signal and said valid indicator (the processor does not

need to invalidate instruction which are not valid) are true.

Note that the conditions for instructions becoming invalidated (said flag being

true) are that the addresses must match and that the CTR bit is opposite from the newly

added entry (match signal) and that the instruction is valid (valid signal).

18.　Regarding claim 14, Eberly/Johnson discloses the apparatus of claim 13,

wherein said invalidation logic invalidates said one of said more than one valid ways of

said selected set if said flag is true (see page 85, last 5 lines).

Note that if all of those conditions are met, the older entries are invalidated.

19.　Regarding claim 15, Eberly discloses a pipelined microprocessor; comprising a

branch target address cache (BTAC), for generating a plurality of indicators in response

to and address (address of newly added entry in the BTAC; see page 84, last 2 lines),

each of said plurality of indicators (indicators must exist if the condition is detected)

indicating whether a corresponding entries in a set of said BTAC selected by said

address is storing a valid target address of said branch instruction (see page 85, last 4

lines regarding determining if address tags are the same);

and logic, coupled to said BTAC, configured to invalidate one or more of said

plurality of entries of said selected set if said plurality of indicators indicates two or more

of said plurality of ways is storing a valid target address of said branch instruction (see

page 85, last 2 lines regarding invalidating all entries with the same address tag and

CTR bit = 1).

Eberly does not expressly disclose an instruction cache, having an address input

for receiving an address to select a line including said branch instruction or that the

BTAC is coupled to said instruction cache. Eberly also doe not expressly disclose that

each entry in the BTAC are ways.

Examiner asserts that it is well known in the art to use an instruction cache

having an address input to select a line to fetch instructions (including branch

instructions). It would have been obvious at the time of the invention for one of ordinary

skill in the art to modify the invention of Eberly by fetching instructions from a cache in

order to decrease access time.

Johnson teaches the use of a set associative cache (see col. 2, lines 30-32) with

multiple sets (see col. 2, lines 30-32), further split into multiple ways (33-36).

For motivation to combine, see above regarding claim 1.

20.   Regarding claim 19, Eberly/Johnson discloses a method for invalidating

redundant entries in a set-associative branch target address cache (BTAC) for the same

branch instruction, the method comprising: determining whether a tag of more than one

way of a set of the BTAC selected by an index portion of an instruction cache fetch

address (see above regarding claim 1) matches a tag portion of the instruction cache

fetch address (see above regarding claim 7) and is valid (only valid instruction need to

be invalidated); and invalidating all but one way of the selected set, if more than one

way of the selected set is valid and matching.

21.　　Regarding claim 20, Eberly/Johnson discloses the method of claim 19, further

comprising: storing an indication that a tag of more than one way of a set of the BTAC

selected by an index portion of an instruction cache fetch address (see above regarding

claim 3) matches a tag portion of the instruction cache fetch address and is valid in

response to said determining (see above regarding claim 7).

22.　　Regarding claim 21, Eberly/Johnson discloses the method of claim 19, further

comprising: storing said instruction cache fetch address, in response to said

determining (see page 84, last 2 lines).

　　　　Note that the CAM is accessed by using a fetch address. Therefore, to invalidate

entries in the CAM, the fetch address would have to be used to access the entries. If

this information is used, it must be stored (even if it is for less than one clock cycle).

23.   Regarding claim 22, Eberly/Johnson discloses the method of claim 19, further

comprising: storing an indication of said all but one way of the selected set that are to

be invalidated, in response to said determining.

Note that in whatever hardware invalidates the entries in the BTAC, an indication

of which ones need to be invalidated must be used. If this information is used, it must

be stored (even if it is for less than one clock cycle).

24.   Claim 23 recites similar limitations as claim 19 with the exception of reciting the

additional limitations of selecting the N-way set with a lower portion of an instruction

fetch address and comparing N address tags of N corresponding ways of said N-way

set with an upper portion of said instruction fetch address.

Eberly does not expressly disclose selecting the N-way set with a lower portion of

an instruction fetch address and comparing N address tags of N corresponding ways of

said N-way set with an upper portion of said instruction fetch address.

Johnson teaches selecting the N-way set with a lower portion of an instruction

fetch address (see col. 2, lines 6-8) and comparing N address tags of N corresponding

ways of said N-way set with an upper portion of said instruction fetch address (see col.

2, lines 13-14).

It would have been obvious at the time of the invention for one of ordinary skill in

the art to have modified the combined invention of Eberly/Johnson (see claim above

regarding 19) by selecting the N-way set with a lower portion of an instruction fetch

address and comparing N address tags of N corresponding ways of said N-way set with

an upper portion of said instruction fetch address in order to more increase hit rate

because usually a program usually runs within a small address range.

25.   Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eberly in

view of Johnson and Patterson et al. (Computer Organization & Design The

Hardare/Software Interface) herein referred to as Patterson.

Eberly/Johnson disclose the microprocessor of claim 15, further comprising: a

first pipeline stage, in which said BTAC indicates a miss of said address therein (see

page 84, second paragraph, lines 3-4);

Note that this event must happen during a clock cycle. Further note that the

BTAC must keep track must keep track of this information and therefore must indicate

the information every clock cycle until it is updated.

and a second pipeline stage, subsequent to said first pipeline stage, which

requests said BTAC to write a resolved target address of said branch instruction (see

page 85, lines 8-9)

Note that the branch instruction will not resolve during the same clock cycle as

when the prediction is made because this would render the branch predictor useless.

Therefore, the second clock cycle must be subsequent to the first clock cycle.

Into said one of said plurality of ways specified by said BTAC in said first pipeline

stage.

Johnson does not expressly disclose that the first pipeline stage said BTAC

specifies one of said plurality of ways for storing said target address.

Patterson teaches specifying one of said plurality of ways for storing said target address during the first stage (Address Calculation stage; see page 453, stage 3).

Note that Patterson teaches generating an address (stage 3; see page 453) for a memory access the clock cycle before the memory is accessed (stage 4; see page 455).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the combined invention of Johnson/Eberly (see above regarding claim 16) by calculating which way to update when a miss occurs in a stage before it is actually written in order to increase performance by decreasing clock time and complexity per stage.

26.   Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eberly in view of Johnson, Patterson and Applicant Admitted Prior Art.

Eberly/Johnson/Patterson disclose the microprocessor of claim 16 (see above regarding claim 16).

Eberly/Johnson/Patterson do not expressly disclose that it is possible for a subsequent fetch of said branch instruction from said instruction cache to reach said first stage prior to a previous fetch of said branch instruction reaching said second stage, such that said selected set of said BTAC stores a valid target address of said branch instruction in two or more of said plurality of ways (see Applicant's Background, paragraph 14).

Applicant teaches that it is possible for a subsequent fetch of said branch instruction from said instruction cache to reach said first stage prior to a previous fetch of said branch instruction reaching said second stage, such that said selected set of said BTAC stores a valid target address of said branch instruction in two or more of said plurality of ways (see Background, paragraph 14).

It is possible because of a short loop and a long pipeline. If there are fewer instructions in a loop than there are pipeline stages between when the prediction is made and when it is updated, this can occur.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Eberly by making it possible for a subsequent fetch of said branch instruction from said instruction cache to reach said first stage prior to a previous fetch of said branch instruction reaching said second stage, such that said selected set of said BTAC stores a valid target address of said branch instruction in two or more said plurality of ways, as taught by the Applicant, in order to increase processor frequency by lengthening the pipeline, and shortening the program length by using shorter loops.

Allowable Subject Matter

27.   Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 17 recites the limitation "wherein said first and second pipeline stages are separated by at least three pipeline stages". The prior art does not teach or fairly suggest splitting the way calculation and the updating by at least three pipeline stages.

Conclusion

28.   The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

29.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

JM 3/14/06

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Au2181   3/20/2006